

**IN THE SPECIFICATION:**

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Replace the first full paragraph of Page 5 with the following paragraph.

AI  
With reference to Figure 3, the network switch 12 includes a MAC module 22 including a transmit MAC portion 23 and a receive MAC portion 25, a receive FIFO buffer 27, a queue block 29, the switch fabric 25, an output queue 42, a dequeue block 44, and a transmit FIFO buffer 46. The queue block 29 and the dequeue block 44 are configured to transfer layer 2 information to and from the external buffer memory 28. The external buffer memory 28 receives data from the queue block 29 via a write bus 31 and the switch fabric 25 snoops on the write bus 31.